IN THE CLAIMS:

Listing of claims:

1. (canceled)

2. (currently amended) A method for manufacturing a semiconductor device ~~according to claim 1, further comprising~~, the semiconductor device having a DRAM including a first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a storage node of the first capacitor and a lower electrode of the second capacitor;

(b) simultaneously forming a dielectric layer of the first capacitor and a dielectric layer of the second capacitor;

(c) simultaneously forming a cell plate of the first capacitor and an upper electrode of the second capacitor; and

before the step (a), the step of simultaneously forming a word line that is a component of the DRAM and a connection layer that is located in a common layer of the word line and that electrically connects the lower electrode to another element in the semiconductor device.

3. (currently amended) A method for manufacturing a semiconductor device ~~according to claim 1, further comprising the step of:~~ the semiconductor device having a DRAM including a first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a storage node of the first capacitor and a lower electrode of the second capacitor;

(b) simultaneously forming a dielectric layer of the first capacitor and a dielectric layer of

the second capacitor;

(c) simultaneously forming a cell plate of the first capacitor and an upper electrode of the second capacitor; and

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

4. (original) A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

5. (canceled)

6. (original) A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried simultaneously with step (c), and

wherein an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

7. (canceled)

8. (original) A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

9-15. (canceled)

16. (currently amended) A method ~~according to claim 15, further comprising,~~ for manufacturing a semiconductor device, the semiconductor device having a DRAM including a first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor formed in an analog element region of the semiconductor substrate, the method comprising:

forming a first conducting layer and etching a portion of the first conducting layer to form a storage node of the first capacitor and a lower electrode of the second capacitor;

forming a dielectric layer and etching a portion of the dielectric layer to form a dielectric layer region of the first capacitor and a dielectric layer region of the second capacitor;

forming a second conducting layer and etching a portion of the second conducting layer to form a cell plate of the first capacitor and an upper electrode of the second capacitor; and

prior to forming the storage node of the first capacitor and the lower electrode of the second capacitor, forming an additional conducting layer and etching the additional conducting layer to form a word line that is a component of the DRAM and to form a connection layer that is

located in a common layer of the word line and that is configured to electrically connect the lower electrode to another element in the semiconductor device.

17-18. (canceled)

19. (currently amended) A method for manufacturing a semiconductor device ~~according to claim 15~~, the semiconductor device having a DRAM including a first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor formed in an analog element region of the semiconductor substrate, the method comprising:

forming a first conducting layer and etching a portion of the first conducting layer to form a storage node of the first capacitor and a lower electrode of the second capacitor;

forming a dielectric layer and etching a portion of the dielectric layer to form a dielectric layer region of the first capacitor and a dielectric layer region of the second capacitor; and

forming a second conducting layer and etching a portion of the second conducting layer to form a cell plate of the first capacitor and an upper electrode of the second capacitor;

wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region.

20. (previously presented) A method as in claim 19, further comprising performing at least one ion-implantation of an impurity into part of the second conducting layer prior to the etching a portion of the second conducting layer.

21. (previously presented) A method as in claim 20, wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

22. (previously presented) A method as in claim 19, wherein, prior to the etching a portion of the second conducting layer, an impurity is diffused in a region where the first

resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

23. (previously presented) A method as in claim 19, wherein prior to the etching a portion of the second conducting layer, a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

24-26. (canceled)